

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit comprising:
a processor core;
a configurable peripheral device comprising a configurable logic block having circuitry capable of implementing a plurality of logic functions; [[and]]
a bus connecting said processor core and said configurable peripheral device;
and
a programmable routing matrix coupled to said configurable logic block, said programmable routing matrix coupling signals to and from said configurable logic block.
2. (Original) The integrated circuit of claim 1 wherein said peripheral device is a universal asynchronous receiver transmitter (UART).
3. (Original) The integrated circuit of claim 2 wherein said UART has a fixed baud rate.
4. (Original) The integrated circuit of claim 1 wherein said processor core, said configurable peripheral device and said bus are implemented on a field programmable gate array.
5. (Original) The integrated circuit of claim 1 wherein said peripheral device is a flash memory controller.
6. (Currently Amended) A system allowing a user to select peripheral devices in a programmable logic device, comprising:
a menu system allowing said user to select one of a plurality of configurable peripheral devices;
a processor core;

a configurable peripheral device comprising a configurable logic block having circuitry capable of implementing a plurality of logic functions; [[and]]

a bus connecting said processor core and said configurable peripheral device;
and

a programmable routing matrix coupled to said configurable logic block, said programmable routing matrix coupling signals to and from said configurable logic block.

Claims 7-9. (Cancelled).

10. (Previously Presented) The system of claim 6 wherein said user selectable options comprise at least one of a UART peripheral selector, an Ethernet peripheral selector and a flash memory peripheral selector.

11. (Previously Presented) The system of claim 10 wherein said user selectable options comprise at least one data width size selector responsive to selection of said flash memory peripheral selector.

12. (Previously Presented) The system of claim 10 wherein said user selectable options comprise an error correction selector responsive to selection of said flash memory peripheral selector.

13. (Previously Presented) The system of claim 12 wherein said user selectable options comprise at least one error correction code selector responsive to selection of said error correction selector.

Claim 14. (Cancelled).

15. (New) An integrated circuit comprising:
a processor core;

a configurable peripheral device comprising a configurable logic block having circuitry capable of implementing a plurality of logic functions;

a bus connecting said processor core and said configurable peripheral device;
and

a configurable input-output block coupled to said configurable logic block, said configurable input-output block coupling signals to and from an external device.

16. (New) The integrated circuit of claim 15 wherein said configurable peripheral device comprises a universal asynchronous receiver transmitter having a fixed baud rate.

17. (New) The integrated circuit of claim 15 wherein said configurable logic block comprises a look-up table.

18. (New) The integrated circuit of claim 15 further comprising a programmable routing matrix coupled to said configurable logic block, said programmable routing matrix coupling signals to and from said configurable logic block.

19. (New) An integrated circuit comprising:

a processor core;

a configurable peripheral device comprising a configurable logic block having circuitry capable of implementing a plurality of logic functions, wherein said configurable logic block comprises a lookup table;

a bus connecting said processor core and said configurable peripheral device.

20. (New) The integrated circuit of claim 19 wherein said configurable peripheral device comprises a universal asynchronous receiver transmitter having a fixed baud rate.

21. (New) The integrated circuit of claim 19 further comprising a configurable input-output block coupled to said configurable logic block, said configurable input-output block coupling signals to and from an external device.

22. (New) The integrated circuit of claim 21 further comprising a programmable routing matrix coupled to said configurable logic block, said programmable routing matrix coupling signals to and from said configurable logic block.